

<b>Form PTO-1449</b> (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5681-03600  APPLICANT: Frankel, et al.  FILING DATE: November 9, 2001	SERIAL NO. 10/007,816  GROUP: 2151
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**U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
DS	B1	6,711,411	3/23/04	Ruffini			
DS	B2	6,134,234	10/17/00	Kapanen			
DS	B3	5,398,317	3/14/95	Nugent			
DS	B4	5,907,685	5/25/99	Douceur			
DS	B5	6,748,451	6/8/04	Woods et al.			
DS	B6	5,875,179	2/23/99	Tikalsky			
DS	B7	5,892,957	4/6/99	Normoyle et al.			
DS	B8	5,991,533	11/1999	Sano et al.			

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

DS	B9	Jerry Banks, ed.; Handbook of Simulation; 1998; John Wiley & Sons, Inc.; pages 3-51
DS	B10	Robert W. Sebesta, Concepts of Programming Language, 1999 Addison Wesley Longman, Inc., Fourth Edition, pages 105-131

EXAMINER:

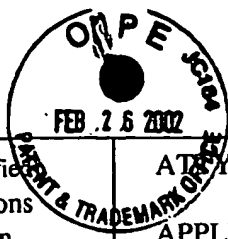
David Silver

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Information Disclosure Statement--PTO 1449 (modified)



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List of Patents and Publications  
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ATTY. DKT. NO. 5681-03600

SERIAL NO. 10/007,816

APPLICANT: Frankel, et al.

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**U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
DS	A1	5,812,824	9/22/98	Dearth, et al.			
DS	A2	5,732,247	3/24/98	Dearth, et al.			
DS	A3	5,881,267	3/9/99	Dearth, et al.			
DS	A4	5,848,236	12/8/98	Dearth, et al.			
DS	A5	6,031,987	2/29/00	Damani, et al.			
DS	A6	5,910,903	6/8/99	Feinberg, et al.			
DS	A7	5,850,345	12/15/98	Son			
DS	A8	6,053,947	4/25/00	Parson			
DS	A9	5,870,585	2/9/99	Stapleton			
DS	A10	5,751,941	5/12/98	Hinds, et al.			
DS	A11	5,634,010	5/27/97	Ciscon, et al.			
DS	A12	6,117,181	9/12/00	Dearth, et al.			
DS	A13	5,519,848	5/21/96	Wloka, et al.			
DS	A14	5,442,772	8/15/95	Childs, et al.			
DS	A15	5,339,435	8/19/94	Lukin, et al.			
DS	A16	4,456,994	6/26/84	Segarra			
DS	A17	5,625,580	4/29/97	Read, et al.			
DS	A18	5,715,184	2/3/98	Tyler, et al.			
DS	A19	5,794,005	8/11/98	Steinman			
DS	A20	5,907,695	5/25/99	Dearth			
DS	A21	4,821,173	4/11/89	Young, et al.			
DS	A22	4,937,173	6/26/90	Kanda, et al.			
DS	A23	5,185,865	2/9/93	Pugh			
DS	A24	5,327,361	7/5/94	Long, et al.			
DS	A25	5,455,928	10/3/95	Herlitz			
DS	A26	6,345,242	2/5/02	Dearth, et al.			

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Information Disclosure Statement--PTO 1449 (modified)

<b>Form PTO-1449</b> (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)		PATENT & TRADEMARK OFFICE FEB 26 2002 ACTY. DKT. NO. 5681-03600 APPLICANT: Frankel, et al. FILING DATE: November 9, 2001	SERIAL NO. 10/007,816 GROUP: 2151
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>			
/	A28	"Rule Base Driven Conversion of an Object Oriented Design Structure Into Standard Hardware Description Languages," Verschueren, A.C., IEEE Xplore, appears in Euromicro Conference, 1998, Proceedings. 24 <sup>th</sup> , vol. 1, August 25, 1998, pages 42-45.	
/	A29	"Modeling Communication with Objective VHDL," Putzke, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 83-89.	
/	A30	"A Procedural Language Interface for VHDL and its Typical Applications," Martinolle, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 32-38.	
/	A31	"The Verilog Procedural Interface for the Verilog Hardware Description Language," Dawson, et al., IEEE Xplore, appears in Verilog HDL Conference, 1996, Proceedings., 1996 International, February 26, 1996, pages 17-23.	
/	A32	"An Integrated Environment for HDL Verification," York, et al., IEEE Xplore, appears in Verilog HDL Conference, 1995, Proceedings., 1995 International, March 27, 1995, pages 9-18.	
/	A33	"The PowerPC 603 C++ Verilog Interface Model," Voith, R.P., IEEE Xplore, appears in Compcon Spring 94, Digest of Papers, Feb. 28, 1994, pages 337-340.	
/	A34	"Networked Object Oriented Verification with C++ and Verilog, Dearth, et al., IEEE, XP-002144328, 1998, 4 pages.	
/	A35	Patent Abstracts of Japan, publication no. 10326835, published December 8, 1998.	
/	A36	Patent Abstracts of Japan, publication no. 10049560, published February 20, 1998.	
/	A37	Patent Abstracts of Japan, publication no. 10340283, published December 22, 1998.	
/	A38	Patent Abstracts of Japan, publication no. 07254008, published October 3, 1995.	
/	A39	"Multiprocessing Verilog Simulator Exploits the Parallel Nature of HDLs." Lisa Maliniak, Electronic Design, Abstract, May 30, 1994, 1 page.	
/	A40	"It's A Multithreaded World, Part I," Charles J. Northrup, BYTE, May 1992, 7 pages.	
/	A41	"It's a Multithreaded World, Part 2," Charles J. Northrup, BYTE, June 1992, pp. 351-356.	
/	A42	"Weaving a Thread," Shashi Prasad, BYTE, October 1995, pp. 173-174.	
/	A43	"Making Sense of Collaborative Computing," Mark Gibbs, Network World Collaboration, January 10, 1994, 4 pages.	
/	A44	"Parallel Logic Simulation of VLSI Systems," Bailey, et al., ACM Computing Surveys, Vol. 26, No. 3, September 1994, pp. 255-294.	
/	A45	"Multithreaded Languages for Scientific and Technical Computing," Cherri M. Pancake, Proceedings of the IEEE, Vol. 81, No. 2, February 1993, pp. 288-304.	
/	A46	"Distributed Simulation Architecture, SW Environment, Enterprise Server Products," Purdue EE400 Presentation by Freyensee and Frankel, November 9, 2000, 13 pages.	

EXAMINER:

A. Silmy

DATE CONSIDERED:

July 5, 05

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